

University of Toronto, Faculty of Applied Science and Engineering  
Department of Electrical and Computer Engineering  
**ECE 1387 - CAD for Digital Circuit Synthesis and Layout**  
**Assignment #2 – Analytical Placement, Spreading, Power-Aware Placement**

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**Assignment Date:** October 11, 2013  
**Due Date:** 11:59pm, October 27, 2013, by email to Jason.  
**Late Penalty:** -2 marks per day late, with total marks available = 20

You are to write an implementation of an analytical placer (AP) with overlap removal (spreading), investigate two different net models (clique and Bound2Bound), and implement power-aware placement. As described in class, you will formulate the placement problem mathematically as a system of linear equations to be solved. You will use an existing package (UMFPACK) to represent the matrices and vectors, and then to solve the linear system.

Your program should display its results using graphics, as in Assignment #1, using either graphics package on the course website. Your graphics should show the placement results and the connectivity between blocks (rat's nest of wires). Blocks (cells) should appear as points in your placement.

The netlist file input format has *four* sections. The four sections are separated from one another by a -1 appearing by itself on a line. The first section has only a single line X Y, indicating the extent of the placement region in the X and Y dimensions. The second section specifies the blocks to be placed and the connectivity between them. Each line has the following form:

blkname blocknum netnum<sub>1</sub> netnum<sub>2</sub> netnum<sub>3</sub> ... netnum<sub>n</sub> -1

where blkname is the name of the cell, and blocknum is a positive integer giving the number of the cell, and the netnum<sub>i</sub> are the numbers of the nets that are attached to that block. Every block that has the same netnum<sub>i</sub> on its description line is attached. Note that each block may have a different number of nets attached to it. Each line is terminated by a -1.

Example input file:

```
50 50
-1
blk1 1 2 3 4 -1
blk2 2 5 4 -1
blk3 3 5 6 2 -1
blk4 4 6 3 -1
-1
blk1 1 50 0
blk4 4 0 50
-1
2 0.5
3 0.3
4 0.22
5 0.37
6 0.1
-1
```

The first line shows that the placement region spans 50 units in the X and Y dimensions. Moving onto the second section, observe that block 1 (called "blk1") is connected to nets 2, 3 and 4. Note that each net may be connected to

more than two blocks (that is, there are multi-fanout nets). Also, note that net numbers are not related to block numbers.

As discussed in class, the AP formulation requires there to be a set of pre-placed (fixed) cells, usually I/Os. The third section of the netlist file specifies the placement of fixed cells. It has the following form:

```
blkname blocknum x_position y_position
```

In the above example, block 1 is pre-placed at the position with  $x = 50$ ,  $y = 0$ . The list of fixed cells is terminated by a  $-1$  by itself on a line.

Finally, the fourth section gives the *switching activity* of each net as a value between 0 and 1, reflecting the fraction of clock cycles in which each net toggles. In the example above, net 2 toggles in 50% of the cycles (it has a switching activity of 0.5). Recall that in CMOS circuits, the power dissipated by a net is proportional to the net's capacitance times its switching activity ( $Power \propto \sum_{i \in nets} Capacitance(i) * Activity(i)$ ).

You should run your placer on the **four** test circuits provided on the course web page.

### What to do and what to hand in?

Hand in the location of the executable. Provide instructions on how to run your program. **Make sure to set file and directory permissions so I can access your placer (on ECF or EEGG). Make sure your home directory is accessible.**

You should hand in a short description of the flow of your program, the main routines and what they do. You do not need to explain analytical placement in your write-up; rather, describe (briefly) any techniques/innovations you used or experimented with for each part.

1. Formulate and solve the analytical placement problem. Use the *clique*<sup>1</sup> net model, as described in class. Do not do any overlap removal in this step and do not use the switching activities in the input file. Your program should display the placement and rat's nest (wires between cells) using the graphics package. Hand in a plot of the placement results for each test circuit. Your program should also compute the half-perimeter bounding box wirelength (HPWL) of the placement. Hand in a table showing the HPWL for each placed test circuit.

**NOTE:** You will need to read Section 2 of the UMFPACK quick start guide (on the course web page) to formulate the problem in UMFPACK's sparse matrix format and then solve the system.

2. Repeat #1 using the *Bound2Bound* net model, as described in class and in the SimPL paper on the course website. Continue to refine edge weights, re-formulate, and re-solve the system until the HPWL does not change by more than 1%. Provide a table of HPWL values when the Bound2Bound model is used and report the number of iterations required for convergence. Compare with the HPWL values achieved by using the clique model in step #1.

3. Implement spreading. You may use the SimPL-style spreading, as discussed in class, *or any other technique you wish*. Assume a bin grid size of  $1 \times 1$ . Assume that cells are "points" (i.e. so they cannot straddle bin boundaries) and that cells have unit area (i.e. each bin of the placement bin grid is intended to accommodate 1 cell). I suggest you use the Bound2Bound net model, however, you may use the clique model if you prefer.

Given a contiguous cluster of over-utilized bins, you have a choice for how to "spread" them into the expanded region R. (as SimPL does). You may implement the recursive alternating vertical/horizontal cut-based spreading, as described in class and in the SimPL paper. Or alternately, you may implement *any* spreading method of your own choosing to distribute cells in the expanded region R.

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<sup>1</sup> In the clique model, a net with  $p$  pins is represented as a complete graph (clique) with  $p(p-1)/2$  edges. Each edge in the complete graph has weight of  $2/p$ . For example, a net with 2 pins has 1 edge with edge weight = 1. A net with 4 pins has 6 edges with edge weight =  $2/4$ .

Given a legalized placement (with  $\leq 1$  cell per bin), introduce weighted pseudo nets into the math formulation. Update the Bound2Bound net model weights (if you used that model) and re-solve the formulation. Iterate the spreading, pseudo-nets introduction, and net model updates as you gradually increase the weights on the pseudo nets. You can implement the weight-increase scheme in the SimPL paper, or any other scheme you find to be effective.

Let  $Q$  represent the set of all bins in the placement bin grid. Compute the overlap of the *solved* placement (i.e. prior to legalization):

$$Overlap = \frac{\sum_{r \in Q} \max(0, m_r - 1)}{m}$$

where  $m$  is the total number of *moveable* cells, and  $m_r$  is the number of *moveable* cells placed in bin  $r$ .  $m_r$  should be computed assuming that cells are points. The intuition behind the above equation is that each 1x1 region can accommodate one cell. I suggest that you aim to spread each test circuit until *solved* Overlap is under 20%.

Report the HPWL for the final solved placement and also for the legalized placement (where there is no more than one cell placed in each bin). Remember that you should *not* include the lengths of the pseudo nets in your HPWL values! Hand in a plot of the placement results, showing the progression of spreading for each circuit and the final spread placement (showing a few intermediate placements is enough). Describe the approach you used for spreading and any innovations you implemented.

4. Implement power-aware placement. Adjust net weights based on the switching activities in the input file, perform spreading, and then compute an estimate of the “power” consumed by the legal placement as follows:

$$Power = \sum_{i \in nets} HPWL(i) * SA(i)$$

where  $SA(i)$  is the switching activity of net  $i$  from the input file. The equation above approximates the routed capacitance of a net by its half-perimeter wirelength. For each circuit, report the HPWL of the solved and legal placement, Power of the solved and legal placement, and the overlap achieved. In your report, describe the approach you used to adjust net weights to optimize power consumption.